FIG.10   CONVENTIONAL ART

Generation of CDFG	S1
Scheduling	S2
Allocation	S3
Generation of data path	S4
Generation of controller	S5

FIG.11   CONVENTIONAL ART

$$x = a \times b + b \times c$$

FIG.12

a   b   c

1 ⓧ   ⓧ 2

CONVENTIONAL ART

+ 3

X

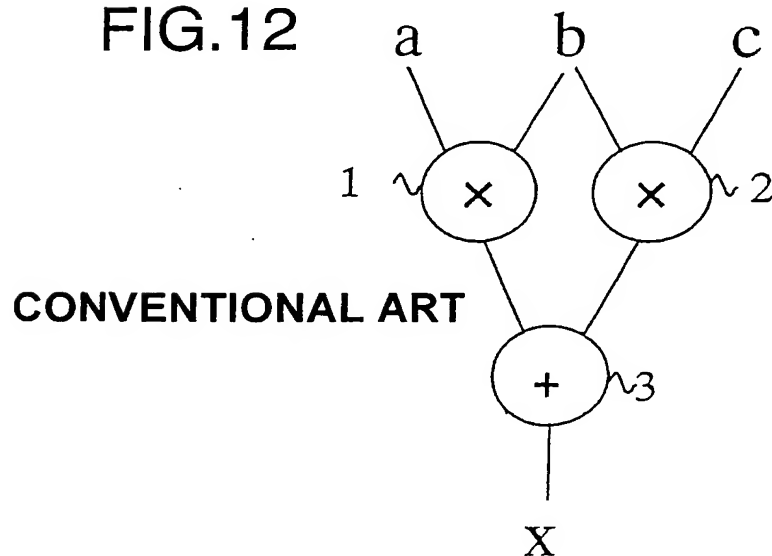## FIG.13

```
struct Node
  {
    int    node_id;
    int    in_edge[2];
    int    out_edge[1];
    int    op_type;
  }
struct Edge
  {
    int    edge_id;
    int    from_node;
    int    to_node;
  }
```
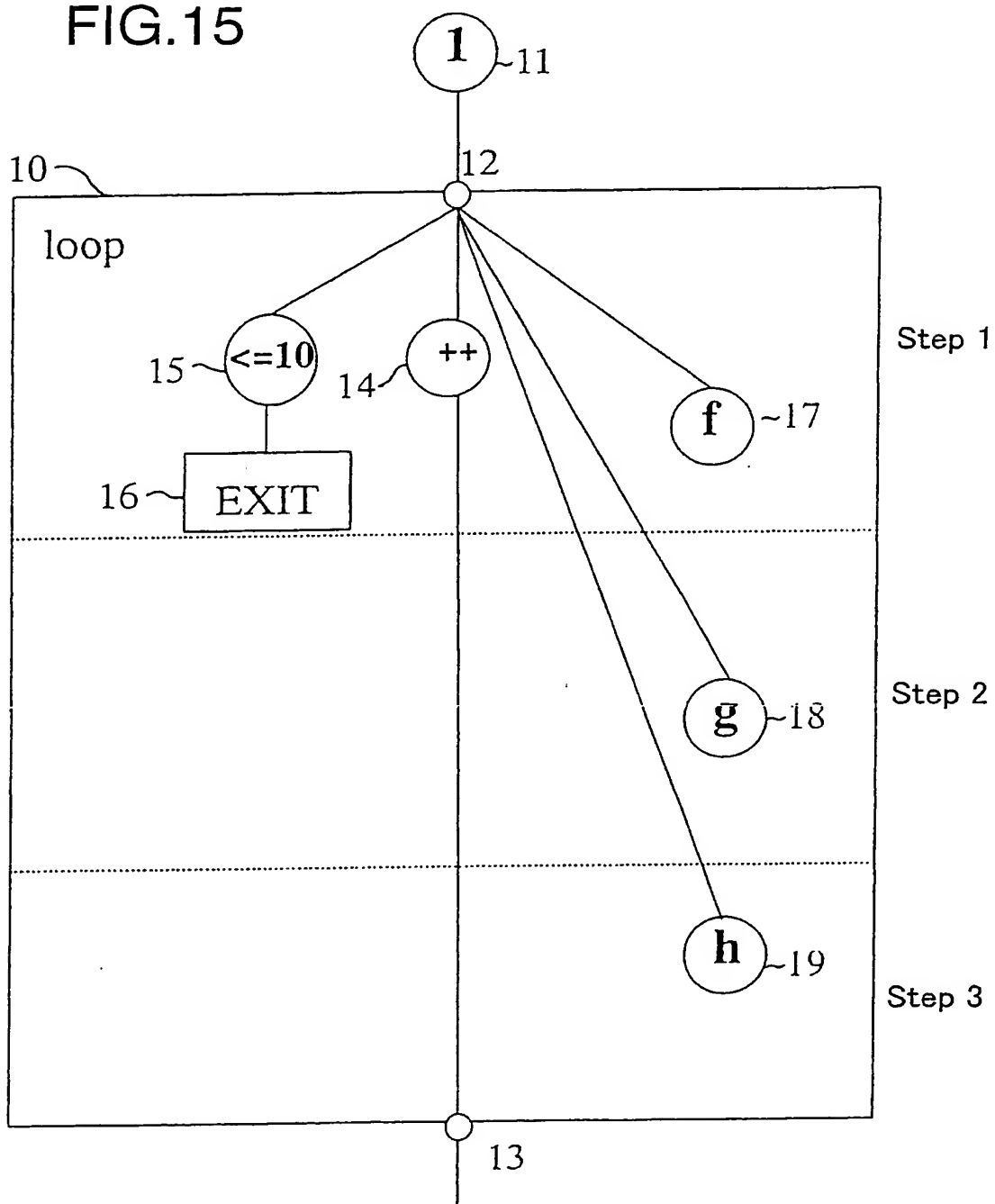
CONVENTIONAL ART

FIG.14

CONVENTIONAL ART

```
for( i =0; i <=10 ; i++)
{
    f(i);
    g(i);
    h(i);
}
```

FIG.15

CONVENTIONAL ART

FIG.16

CONVENTIONAL ART

Cycle 1			f(1)
Cycle 2		g(1)	f(2)
Cycle 3	h(1)	g(2)	f(3)
Cycle 4	h(2)	g(3)	f(4)

Cycle 9	h(7)	g(8)	f(9)
Cycle 10	h(8)	g(9)	f(10)
Cycle 11		h(9)	g(10)
Cycle 12			h(10)

FIG.17   CONVENTIONAL ART